

ABSTRACT

A method for designing a system on a target device utilizing field programmable gate arrays (FPGAs) includes identifying a group of components associated with a critical signal in the system. A first copy and a second copy of the group of components are generated where the first
5 copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state. The system is configured to select an output of one of the first copy and the second copy in response to the critical signal.